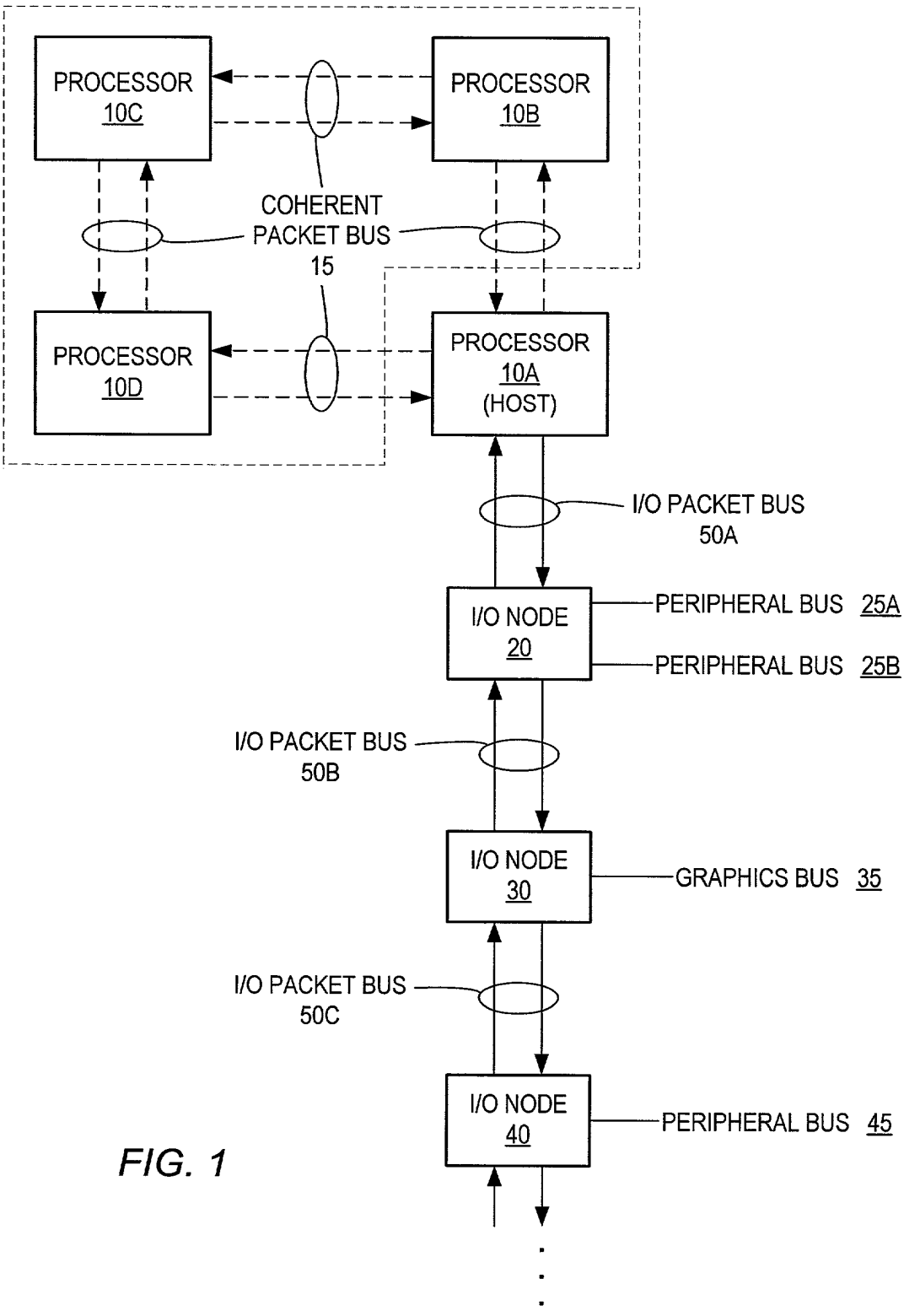
PROCESSOR
10C
PROCESSOR
10B
COHERENT
PACKET BUS
15
PROCESSOR
10D
PROCESSOR
10A
(HOST)
I/O PACKET BUS
50A
I/O NODE
20
PERIPHERAL BUS 25A
PERIPHERAL BUS 25B
I/O PACKET BUS
50B
I/O NODE
30
GRAPHICS BUS 35
I/O PACKET BUS
50C
I/O NODE
40
PERIPHERAL BUS 45

FIG. 1

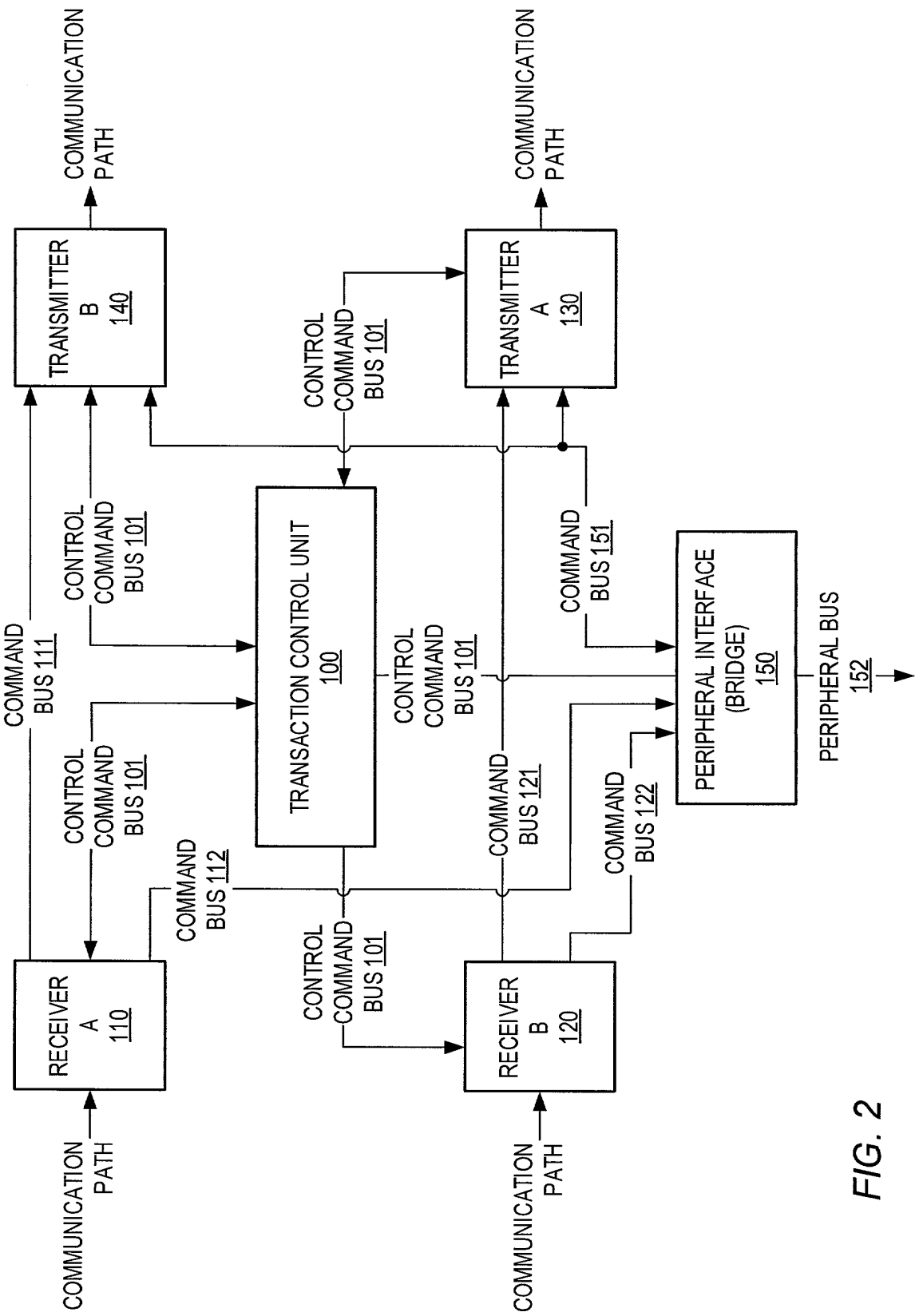
COMMUNICATION PATH
RECEIVER A 110
COMMUNICATION PATH
TRANSMITTER B 140
COMMUNICATION PATH
RECEIVER B 120
TRANSMITTER A 130
COMMUNICATION PATH
COMMAND BUS 111
CONTROL COMMAND BUS 101
CONTROL COMMAND BUS 101
CONTROL COMMAND BUS 101
CONTROL COMMAND BUS 101
TRANSACTION CONTROL UNIT 100
COMMAND BUS 112
COMMAND BUS 121
COMMAND BUS 122
COMMAND BUS 151
PERIPHERAL INTERFACE (BRIDGE) 150
PERIPHERAL BUS 152

FIG. 2

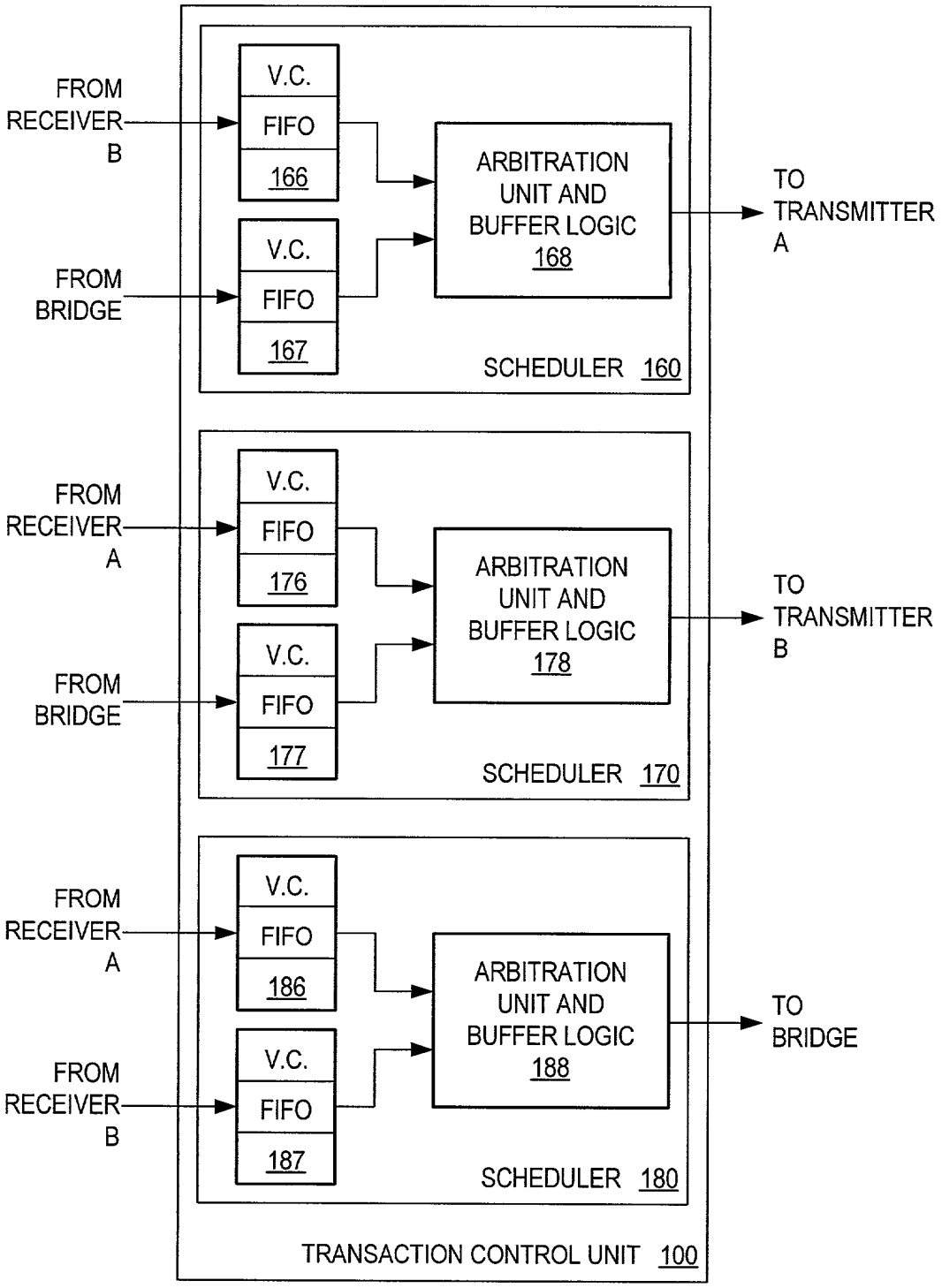
FROM RECEIVER B
V.C.
FIFO
166
FROM BRIDGE
V.C.
FIFO
167
ARBITRATION UNIT AND BUFFER LOGIC 168
TO TRANSMITTER A
SCHEDULER 160
FROM RECEIVER A
V.C.
FIFO
176
FROM BRIDGE
V.C.
FIFO
177
ARBITRATION UNIT AND BUFFER LOGIC 178
TO TRANSMITTER B
SCHEDULER 170
FROM RECEIVER A
V.C.
FIFO
186
FROM RECEIVER B
V.C.
FIFO
187
ARBITRATION UNIT AND BUFFER LOGIC 188
TO BRIDGE
SCHEDULER 180
TRANSACTION CONTROL UNIT 100

FIG. 3

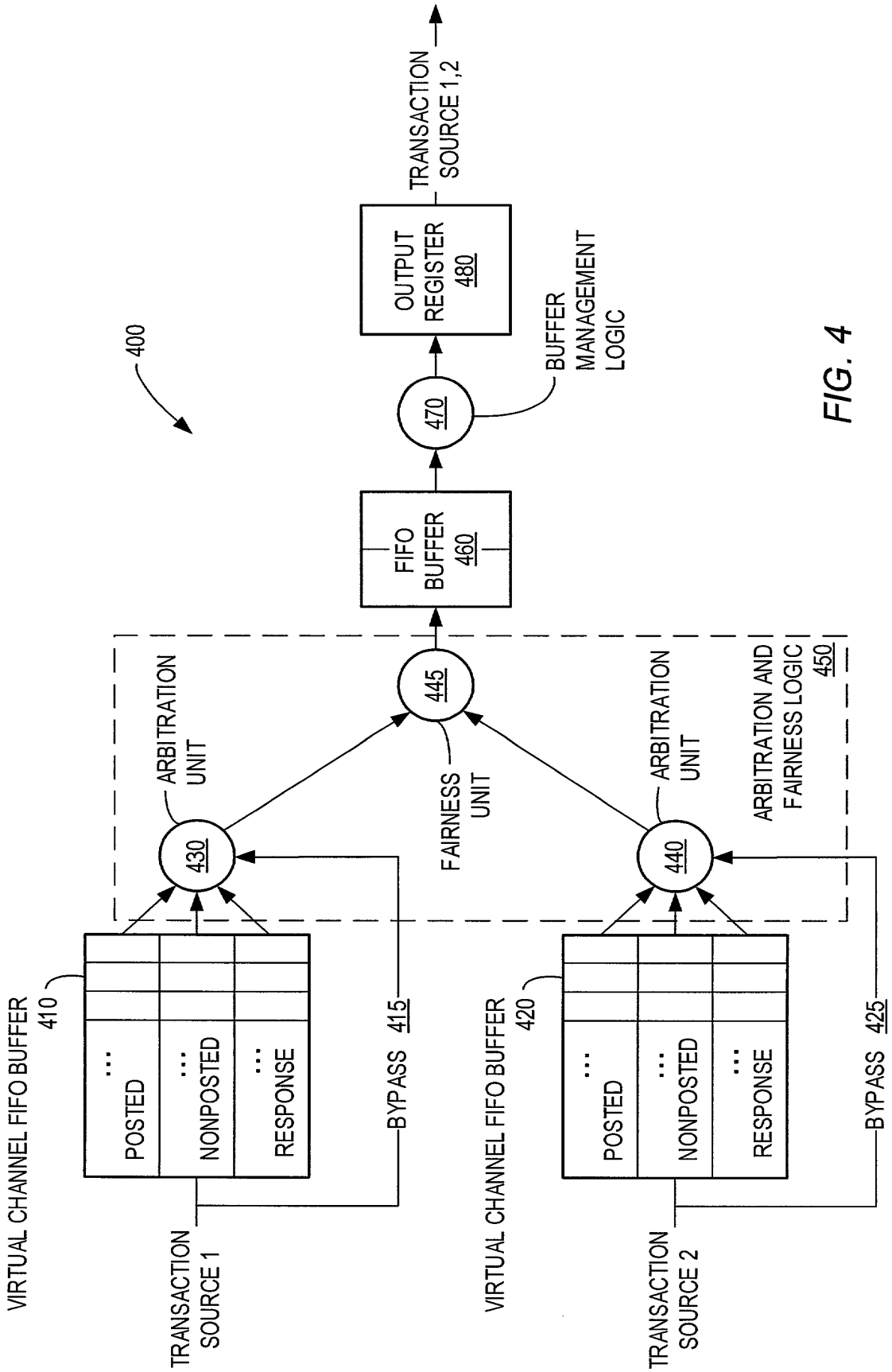
400
VIRTUAL CHANNEL FIFO BUFFER 410
POSTED
NONPOSTED
RESPONSE
TRANSACTION SOURCE 1
BYPASS 415
VIRTUAL CHANNEL FIFO BUFFER 420
POSTED
NONPOSTED
RESPONSE
TRANSACTION SOURCE 2
BYPASS 425
ARBITRATION UNIT
430
ARBITRATION UNIT
440
FAIRNESS UNIT
445
ARBITRATION AND FAIRNESS LOGIC 450
FIFO BUFFER 460
470
BUFFER MANAGEMENT LOGIC
OUTPUT REGISTER 480
TRANSACTION SOURCE 1,2

FIG. 4

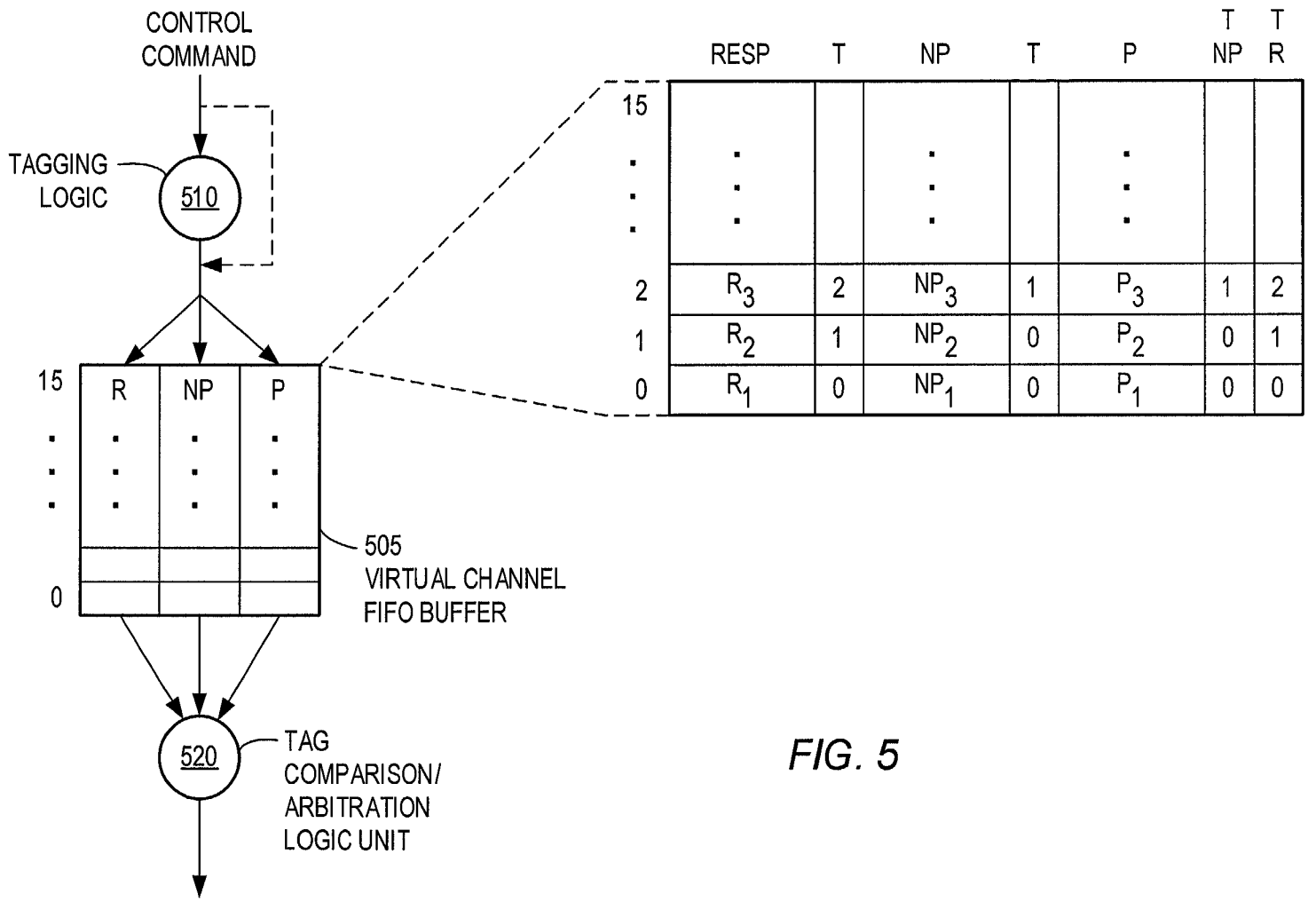
CONTROL COMMAND
TAGGING LOGIC
510
15
0
R
NP
P
505
VIRTUAL CHANNEL FIFO BUFFER
520
TAG COMPARISON/ ARBITRATION LOGIC UNIT
RESP
T
NP
T
P
T NP
T R
15
2
1
0
R_3
2
NP_3
1
P_3
1
2
R_2
1
NP_2
0
P_2
0
1
R_1
0
NP_1
0
P_1
0
0

FIG. 5

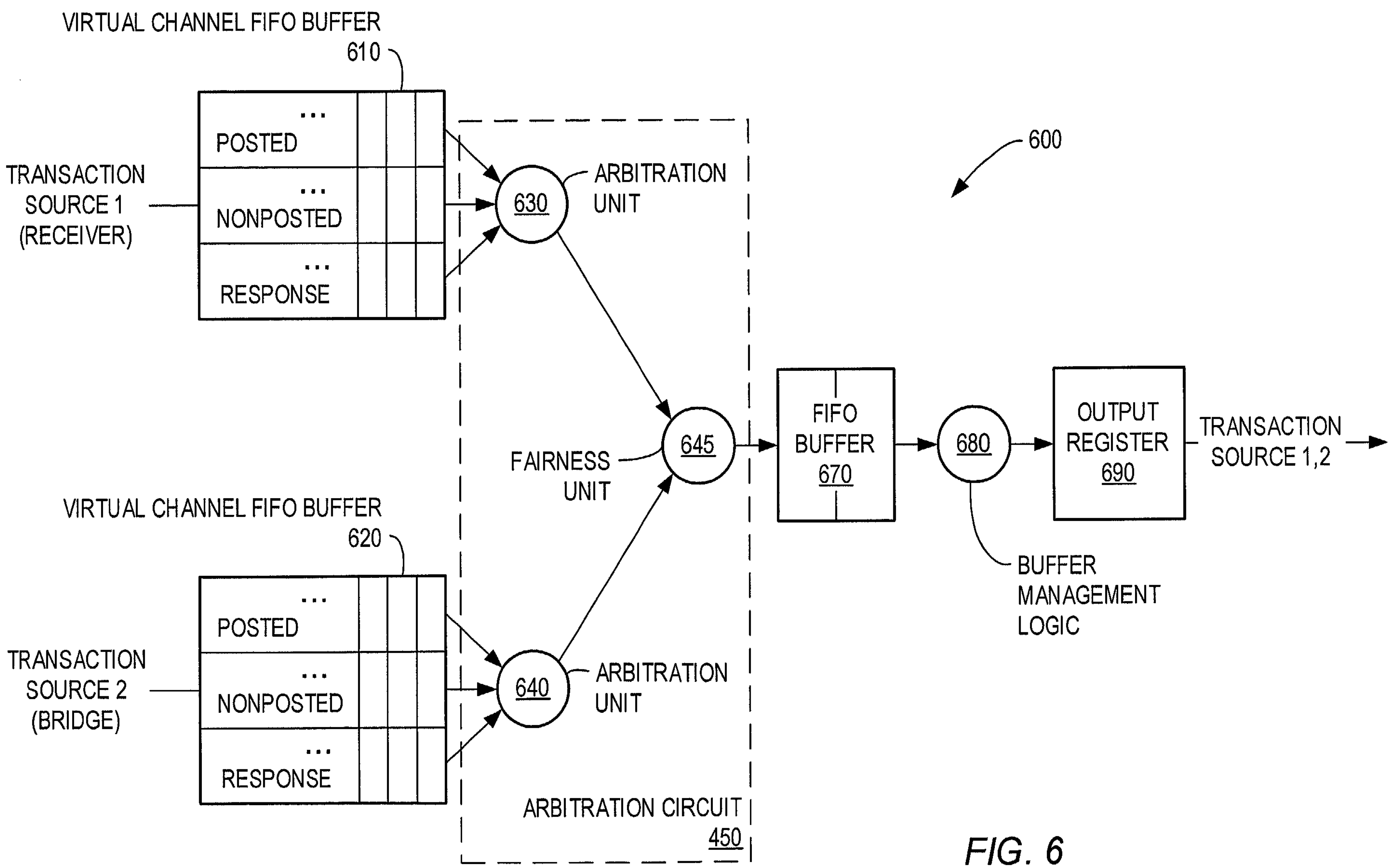
VIRTUAL CHANNEL FIFO BUFFER
610
TRANSACTION SOURCE 1 (RECEIVER)
POSTED
NONPOSTED
RESPONSE
VIRTUAL CHANNEL FIFO BUFFER
620
TRANSACTION SOURCE 2 (BRIDGE)
POSTED
NONPOSTED
RESPONSE
630
ARBITRATION UNIT
640
ARBITRATION UNIT
645
FAIRNESS UNIT
ARBITRATION CIRCUIT
450
600
FIFO BUFFER
670
680
BUFFER MANAGEMENT LOGIC
OUTPUT REGISTER
690
TRANSACTION SOURCE 1,2

FIG. 6

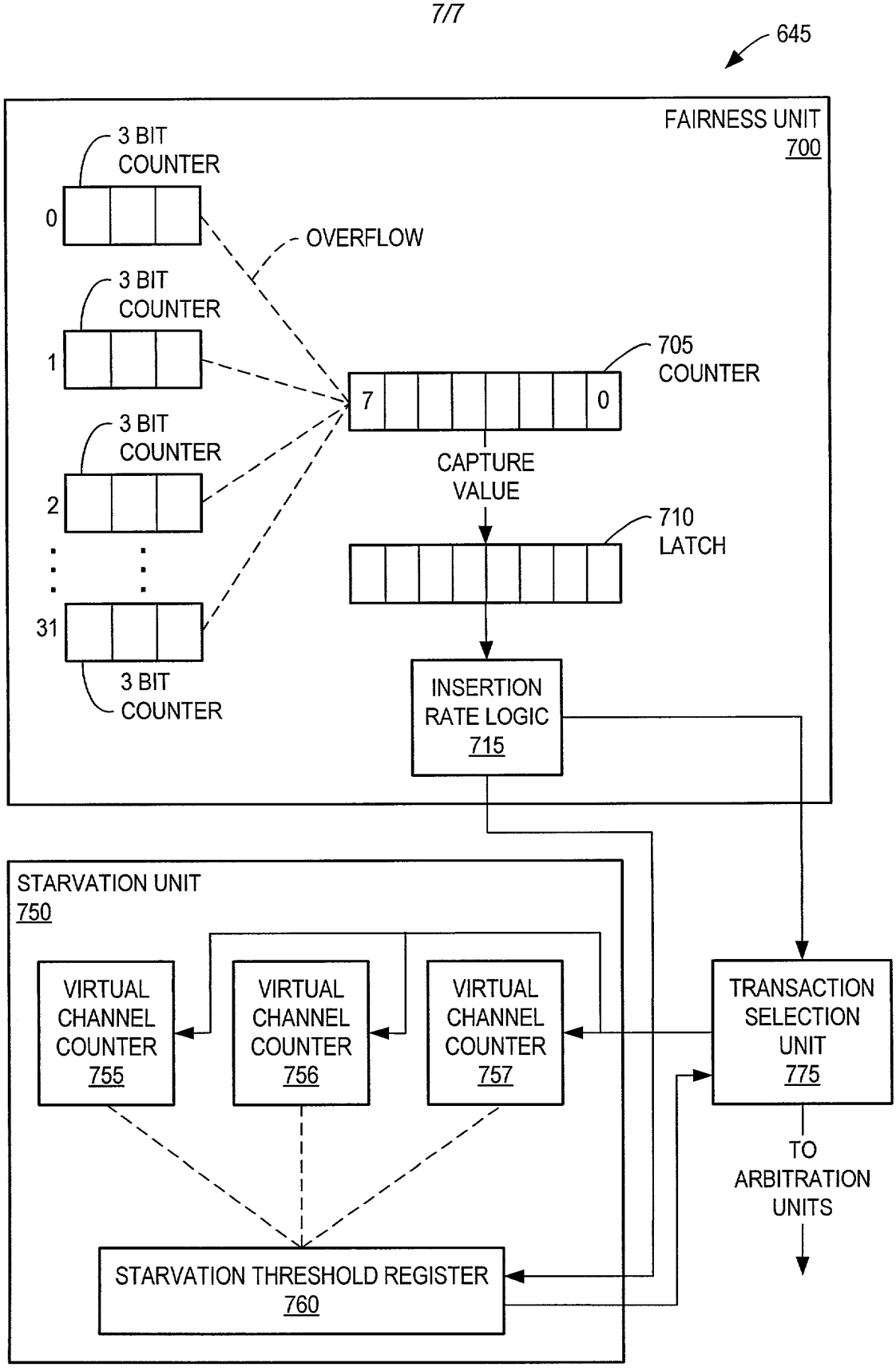
645
FAIRNESS UNIT
700
3 BIT
COUNTER
0
OVERFLOW
3 BIT
COUNTER
1
3 BIT
COUNTER
2
3 BIT
COUNTER
31
705
COUNTER
7
0
CAPTURE
VALUE
710
LATCH
INSERTION
RATE LOGIC
715
STARVATION UNIT
750
VIRTUAL
CHANNEL
COUNTER
755
VIRTUAL
CHANNEL
COUNTER
756
VIRTUAL
CHANNEL
COUNTER
757
TRANSACTION
SELECTION
UNIT
775
TO
ARBITRATION
UNITS
STARVATION THRESHOLD REGISTER
760

FIG. 7